Specification Am ndm nts

Paragraphs at page 2, starting at line 24:

The gate comparator to be described preferably is realized in JAVA® application software running on a Windows®-~~like~~ operating system of a modern oscilloscope.

FIGURE 1 is an illustration of a screen display **100** showing two reference waveforms in a waveform display area **110**, and a gate comparator control panel in a controls area **115**. There are four selectable gate controls (i.e., a measurement window controls), ~~**Ref Gate,**~~ **Gate 1**, **Gate 2**, **Gate 3**, and **Gate 4**. **Gate 1** is considered to be ~~the~~ a reference gate **Ref Gate**. The control panel of FIGURE 1 is used to set the working parameters for **Ref Gate** (and other gates **Gate 2**, **Gate 3**, **Gate 4**, if desired). The waveform display of FIGURE 1 indicates that two gates are active, **Gate 1** and **Gate 2** producing reference waveforms **R1** and **R2,** respectively.

This control screen has "soft keys" for Run **140**, Stop **145**, Pause **150**, and Reset **155** functions, for controlling a "roll mode" that works like a standard tape deck control. Speed selection for the roll mode scan is also provided via ~~and~~ a control **160** for selecting step size.

Paragraph at page 3, starting at line 5:

FIGURE 2 is an illustration showing the effect of turning-on the gate comparator. FIGURE 2 shows the two reference waveforms **R1** and **R2** and display **M1** of the gate comparison regions. When the gate comparator is turned-on, the value of the signal within all other active gates (i.e., other gates that are also turned-on) will be subtracted from the value of the signal within **Gate 1** on a point-by-point basis to produce a difference. This scanning process causes all gates to move together along a signal to maintain their constant space between them.

Paragraph at page 5, starting at line 3:

Another gate comparator control screen display is shown in FIGURE 5. The features of this control screen are as follows. There is a control menu for each of four gates, **Gate 1**, **Gate 2**, **Gate 3**, and **Gate 4**. Each gate menu allows a user to choose a source waveform for the gate and a position for the gate on that waveform. In addition, there is an on/off control for each gate. This control screen also has soft keys for Run, Pause and Stop functions, for controlling a "roll mode" that works like a standard tape deck control. Speed selection for the roll mode scan is also provided via ~~and~~ a control for selecting step size.

Paragraph at page 5, starting at line 19:

Figure 6 is a simplified block diagram of a modern digital oscilloscope **600** useful for practicing the subject invention. It includes an input **601** for acquiring a signal from a circuit under test. The "front end" includes Trigger Circuitry **605** for generating trigger signals to be applied to an Acquisition System **610**. Acquisition System **610** acquires digital signal samples continuously, and in response to triggers signals, stores them in an Acquisition memory **615**. Acquisition memory **615** supplies signal samples to Rasterizer **620** for processing, storage in raster memory **622**, and eventual display. A more analog-like display is obtained by means of the arrangement of a Raster Combiner **625** and Raster Memories **630**, **635** that permits graceful decay of the displayed signals. The output of this arrangement is displayed on a display screen **640** of the oscilloscope. The oscilloscope operates under control of two controllers, a process controller **650**, and a System controller **660**. System controller **660** interfaces with the reference memories REF Memory 1 **REF 1**, REF Memory 2 **REF 2**, REF Memory 3 **REF 3**, and REF Memory 4 **REF 4**.

Paragraph at page 6, starting at line 14:

Although the gate comparator of the subject invention has been described

as preferably being realized in JAVA® application software running on a Windows®-~~like~~ operating system, the invention is not intended to be so restricted, and is intended to encompass hardware circuitry for performing the comparison functions described herein.